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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,155	06/30/2003	Hiroshi Matsushita	239736US2	8151

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

H/A

Office Action Summary	Application No.	Applicant(s)	
	10/608,155	MATSUSHITA, HIROSHI	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-9 and 11-24* is/are pending in the application.

4a) Of the above claim(s) *17-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9 and 11-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/608,155 filed 06/03/2003 and amendment filed 01/31/2006.

2. Claims 1, 2, 4-9 and 11-24 remain pending in the Application. Claims 3 and 10 have been cancelled from the Application. Claims 17-24 have been withdrawn from the consideration.

3. Applicant's arguments have been fully considered but they are not persuasive.

Specification

4. The title of the invention is not descriptive. A new title is required that is **clearly indicative** of the invention to which **the claims are directed**. The title includes a manufacturing method, which is not indicated in the claims in response to the restriction requirement.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 2, 8, 9 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Oda et al. (Japan Patent JP410104314A).

With respect to claims 1, 8 and 16 Oda et al. teaches a failure analysis system, a failure analysis method, a computer program product configured to be executed by a computer within a method of analyzing the wafer failure using wafer failure-analysis

equipment (page 1, paragraph [0005]) using the computer system, which is described by Drawing 1 including all attributes of the computer system, for example: CPU, mouse, display, storage, programming code to be executed (page 1, paragraph [0007]; page 2, paragraph [0013]), comprising: a chip position calculation module configured to calculate fault chip positions of a plurality of circuit blocks in a chip region based on layout information on the circuit blocks positioned in the chip region and fault information on the circuit blocks within wafer failure-analysis equipment depicted on the Drawing 1, wherein operation part 30 is controlled by the operator performs the operations (page 1, paragraph [0007]), the storage section 20 to store various information acquired from integrated circuit testing device (page 2, paragraph [0009]) including a defect information file F for storing the chip information Ci1 and Ci2, such as chip location on the wafer (page 2, paragraph [0009]); a wafer position calculation module configured to calculate fault wafer positions in a wafer based on the fault chip positions and position information showing a chip region layout in a wafer plane within wafer failure-analysis equipment depicted on the Drawing 1, wherein operation part 30 is controlled by the operator performs the operations (page 1, paragraph [0007]), the storage section 20 to store various information acquired from integrated circuit testing device (page 2, paragraph [0009]) including a defect information file F for storing wafer information Wi; and a mapping module configured to perform a mapping display of the fault wafer positions in accordance with physical coordinates on the wafer plane by creation of a fail bit map from the defect information by physical arrangement of the chip formed on the wafer, including the display which displays the fail bit map (page 1,

paragraph[0006; page 2, paragraph [0012]]); an index calculation module configured to calculate fault-extracting-index for extracting a fault mode based on a result of the mapping display as demonstrated by Fig. 11, showing the map, which displayed the fail bit map as a fault-extracting-index, wherein the part of the chip with the fail is smeared away (black) shows the specific fault mode (paragraph [0043]); and an index comparison module configured to compare a threshold of the fault-extracting-index for extracting a specific fault mode to the calculated fault-extracting-index and determines the presence of the specific fault mode within the feature during displaying the fail bit map by showing faulty parts in a red color, i.e. when the limit of faults is reached (exceeding the threshold) (paragraph [0018]) within operation part 30 performing creation of the indicative data and comparison with the fault limit (paragraph [0027]).

With respect to claims 2, 9 Oda et al. teaches:

Claims 2 and 9: wherein the fault information is one of fail bit maps and pass/fail maps of the circuit blocks by creating the map in which the pass/fail for every data bit are shown from the defect information in wafer failure-analysis equipment (page 1, paragraph [0006]);

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4-7, 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oda et al. as applied to claims 1, 3, 8 above in view of Morioka et al. (US Patent 6,611,728).

With respect to claims 4-7, 11-15 Oda et al. teaches the limitations from which the claims depend. However Oda et al. lacks the specifics regarding arc periphery fault. Morioka et al. teaches:

Claims 4 and 11: the fault mode is an arc periphery fault mode as shown on the Fig. 36 (col. 26, ll.38-39);

Claim 5: the arc periphery fault is biased toward a periphery region of the wafer and has a geometric symmetry as shown on the Fig. 36;

Claim 6: a classification module configured to set a hierarchical structure between a plurality of fault-extracting-indices and performs detection and classification of unknown fault modes based on classification information in which the fault-extracting-indices are classified in the hierarchical structure using the image index in the defect location history list including the wafer identification information, such as product name, lot number and wafer number of the wafer and inspection process name (col. 20, ll.45-62; col. 22, ll.49-51) and identification of the defects, including defect coordinates, to avoid a redundancy (col,26, ll.42-45; col. 25, ll.44-47);

Claims 7 and 14: the hierarchical structure includes at least an arc periphery fault, a periphery fault including the arc periphery fault and a cluster fault including the periphery fault as shown on the Fig. 36 (col.26, ll.38-40; col. 10, ll.52-54; col. 22, ll.49-55);

Claim 12: the fault-extracting-index is calculated by a degree of bias of fault densities in a region where the arc periphery fault occurs and by a degree of continuity of the longest continuous faults adjacent two of which is spaced apart by a distance within a threshold in the region where the arc periphery fault occurs within an ability of the inspection system to select any defect whose image is needed by user (col. 26, ll.61-63) with consideration a density of the defects on the wafer including a threshold by indexing the defects (col. 10, ll.52-60; col. 27, ll.1-4).

Claim 13: setting a hierarchical structure between a plurality of fault-extracting-indices within defect location history list including the wafer identification information, such as product name, lot number and wafer number of the wafer and inspection process name (col. 20, ll.45-62) with consideration of the image index (col. 22, ll.49-55) (col.; and performing detection and classification of unknown fault modes based on classification information in which the fault-extracting-indices are classified in the hierarchical structure, and a result of determining the presence of the fault mode for each of the fault-extracting-indices within identification of the defects, including defect coordinates, to avoid a redundancy (col,26, ll.42-45; col. 25, ll.44-47);

Claim 15: the fault mode is classified as the unknown fault mode concerning upper-level fault-extracting-index when it is determined that there is a fault in the upper-level fault-extracting-index of the hierarchical structure and there is no fault in fault-extracting-index one level lower than the upper-level fault-extracting-index by setting a specific index for the defect in the defect location history list (col. 27, ll.8-17).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Morioka et al. to teach the specifics subject matter Oda et al. does not teach, because it's possible to reduce the analyzing time and improve the analyzing accuracy (col. 27, ll.56-57).

Remarks

9. In the remarks Applicant argues in substance:

a) Oda et al. does not include a fault-extracting index or determine the presence of a specific fault mode

b) Oda et al. does not disclose or suggest an index calculation module configured to calculate a scalar or quantity of a fault-extracting-index for extracting a fault mode based on a result of the mapping display and an index comparison module configured to compare a threshold of the fault-extracting-index for extracting a specific fault mode to the calculated scale or quantity of the fault-extracting-index and determine the presence of the specific fault mode

c) Oda et al. does not disclose or suggest features: calculating a scalar quantity of a fault-extracting-index for extracting a fault mode based on a result of the matching display and determining the presence of the fault mode by comparing the scalar quantity of the fault-extracting-index with a threshold stored in a threshold information storage unit and an instruction of calculating a scalar quantity of a fault-extracting-index for extracting a fault mode based on a result of the mapping display and an instruction of determining the presence of the fault mode by comparing the scalar quantity of the false-extracting index with a threshold stored in a threshold information storage unit

10. Examiner respectfully disagrees for the following reasons:

As to a) Oda et al. discloses an improved method for defect analysis by forming a fail bit map at the physical arrangement of a chip formed on a wafer from defect information by an operating part, selecting the chip displayed on the fail bit map and forming the fail bit map at a memory-cell array unit (abstract); moreover, as demonstrated by Fig. 11, showing the **map**, which **displayed the fail bit map** as a fault-extracting-index, wherein the part of the chip with the **fail is smeared away** (black) shows the specific fault mode (paragraph [0043]).

As to b) Oda et al. discloses analyzing and displaying the fail bit map (paragraph [0003]) using failure-analysis equipment (paragraph [0006]) within the computer system demonstrated by the Fig. 1, wherein operation part 30 performs the operation of generating and analyzing the fail bit map including **calculation** of the physical relationship of each chip and a wafer (for displaying the fail bit map of a wafer scale) (paragraph [001]) with further displaying the result (an indicative data) of an operation of operation part 30 on a display 40 (paragraph [0007]) using classification-by-color during displaying the fail bit map (paragraph [0011]), which shows statistics of occurrence frequency of the fault (paragraph [0021]).

As to c) Oda et al. discloses the system shown on the Fig. 1 performing analysis and display the fail bit map (paragraph [0003]), including the feature during displaying the fail bit map by showing faulty parts in a red color, i.e. when the **limit** of faults is reached (exceeding the threshold) (paragraph [0018]) within operation part 30

performing creation of the indicative data and comparison with the fault **limit** (paragraph [0027]).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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